REMARKS

Claims 8, 10-13, 15-24, 28-35, and 37-42 remain in this application. Claims 8, 10-11, 19-22, 28-29, 31, 34, 37, and 39 are amended by this amendment.

Replacement sheets for the drawings of Figs. 1-3, with enlarged reference numbers are enclosed.

The claim amendments correct the informalities noted by the Examiner. However, the objection to claim 32 could not be found, although an error of this type was corrected in claim 34. The error noted in paragraph 13 (claim 34) could not be found. Claims 20 -21 are amended to provide proper antecedent basis and, thus, the rejection of claims 20-24 as indefinite will be overcome with entry of this amendment. Since these amendments only relate to formal matters entry at this time is proper. The Examiner rejected claim 38 as indefinite but gave no reason. Applicants submit that this claim is definite.

All claims are rejected as obvious over Blomgren et al. in view of Yeager et al., with claims 38-42 rejected over this combination and further in view of Shippy. Applicants respectfully traverse these rejections. The Examiner admits that Blomgren does not teach renaming of registers, but asserts that teaching of such in Yeager makes it obvious to modify Blomgren to have register renaming. However, Yeager, prior to renaming, does not have a result register that is the same as one of the source registers. Applicants submit that, because of this one would not be motivated to combine Yeager's teaching with Blomgren, which does have a destination register that is the same as one of the source registers. Alternatively, combining these two references one would have an arrangement where the original registers, before renaming would have a separate result register as in Yeager. Furthermore, where does one find any suggestion of or motivation for combination in either reference? Applicants submits such suggestion of combining these features comes only from his specification and that the Examiner is engaging in hindsight reconstruction.

The Examiner also refers to knowledge in the art regarding the benefits of register renaming. In view of this, it is not clear to Applicants if the Examiner finds Yeager to suggest modifying Blomgren or if he contends the suggestion comes from what is alleged to be well-known art. Applicants submit that this is not the type of fact of which notice can be taken. If the Examiner wishes to rely on this fact, he should cite a reference with the appropriate teaching. Beyond that, if this is so well known and obvious to do, why didn't Blomgren do it? In view of these deficiencies, Applicants believe that all remaining claims should be allowed.

In addition, even if the combination of references is considered proper, limitations are still missing. As seen in Fig. 6, the renamed registers 550 and 560 have low order bits and high order bits. In claim 6, the instruction is carried out on the values in the registers. Thus, both high order and low order bits are added. In the example that the Examiner says meets this limitation, BH and AL are added. But BH has only high order bits and AL low order bits. Furthermore, passing the bits of the top and high adders does not equate to the steps of modifying or identifying. Again the adding that takes place is only of bits 7:0 of operand A and 15:8 of operand B in the adder 164. There is no adding the operands of two source registers having high and low order bits. It is adding the lower order bits form one register to higher order bits of another register. Note that the patent in Fig. 2 does not care about the results of the addition of the lower order bits in adder 162. Applicants submit that this reference does not teach what is called for in the claims.

Claim 11 further requires "preventing the propagation of a carryover of a result of the executed instruction from low-order bit positions of a renamed result register to high-order bit positions of the renamed result register; and." The other independent claims have similar limitations. The teaching in Blomgren relied upon by the Examiner is the following at col. 11, lines 25-30: "Mixed-alignment byte adders need not generate carries to larger size adders because mixed-alignment only occurs with byte addition. Therefore, FIG. 2 depicts generate/propagate paths only from the fixed-alignment adders to upper adders." In other words, adders 164 and 166 have no generate/propagate paths while adders 162 and 168 do.

Various claims have further distinguishing feature that will now be discussed.

Regarding claim 19, Applicants see nothing in the portions of Blomgren cited that make reference to the claimed logic circuit. Fig. 2 only shows adders and multiplexers; nothing of the nature of the circuit shown in Applicants' Fig. 6, to which the logic circuit limitation is directed is shown or suggested. In particular, there is no teaching of the claimed carryover circuit. Thus, claim 19 and claims dependent thereon are more clearly allowable.

Regarding claims 28 and 31, Applicants note the following. As previously discussed, the claimed renamed source registers have high order bits and low order bits. In this claim the high order bits of one are designated to stay the same and the high order bits of the other set to zero. The contents of the two source registers including high and low order bits are added and a carryover from the low order bits is prevented.

Again the Examiner argues that the example where BH and AL are added meets this limitation. But, as previously noted, BH has only high order bits and AL low order bits. Passing the bits of the top and high adders does not equate to the steps of modifying or identifying. The adding that takes place is only of bits 7:0 of operand A and 15:8 of operand B in the adder 164. There is no adding the operands of two source registers having high and low order bits. In view of these differences, claims 28 and 31 further distinguish over the art and are more clearly allowable.

Looking at claim 29 and 32, we can see that again both renamed source registers have high and low bits. In one, low order bits are set to zero and in the other the high order bits set to zero. At Col. 9, line 64 to col. 10, line 10 of Blomgren, an 8-bit operation is described. This involves only low order bits. There is no description of setting low order bits in one and high order bits in the other renamed source register to zero. Thus, these claims and claims 30 and 33 dependent thereon are further allowable for these additional reasons.

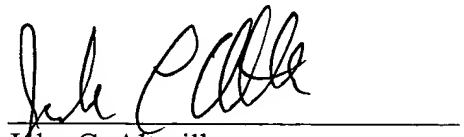
Turning to claims 38-42, the comment above about the lack of clear teaching of what is claimed at Blomgren col. 11, lines 25-29 is noted. The Examiner says Blomgren does not say how he turns the carryover on or off. However, it is clear that Blomgren does not teach turning it on or off. Rather, for some adders carryover is provided and for others it is not. Thus, these claims are further allowable for the above reasons.

In view of the differences noted above, Applicants submit that, as now presented, with entry of this amendment to correct formal matters, all remaining claims distinguish over the art and are in condition for allowance. Thus, entry of this amendment and prompt notice of allowance is respectfully solicited.

The Examiner is invited to call the undersigned at (202) 220-4200 to discuss any information concerning this application.

The Office is hereby authorized to charge any additional fees under 37 C.F.R. § 1.16 or § 1.17 or credit any overpayment to Deposit Account No. 11-0600.

Respectfully submitted,



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John C. Altmiller
Registration No. 25,951

KENYON & KENYON
1500 K Street, N.W., Suite 700
Washington, D.C. 20005
Tel.: (202) 220-4200
Fax.: (202) 220-4201
606901_1.DOC